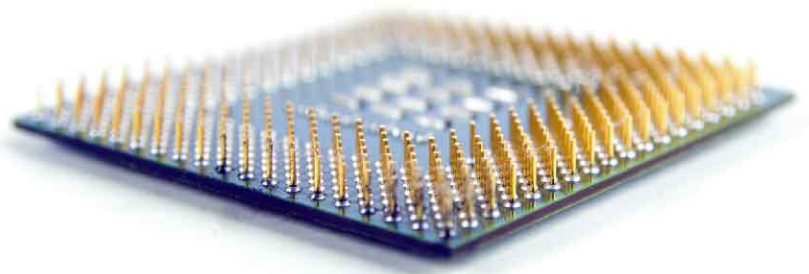


FloorDirector®

Early Stage Dynamic Power Optimization
Lower IR Drop, EMI and Noise

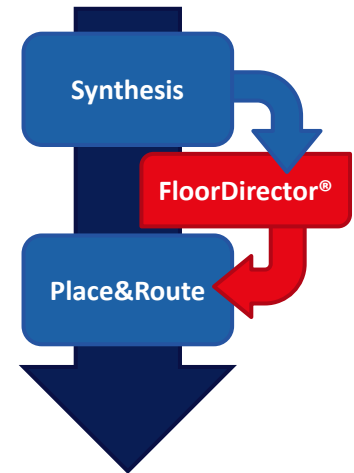


FloorDirector®

Complex System-on-Chip (SoC) designs at deep submicron geometries suffer from increasing power grid noise and IR drop due to dynamic supply currents with high peaks and steep slopes. Particularly ICs for highly integrated portable and automotive applications, as well as RF and mixed-signal ICs with noise-sensitive analog blocks, are suffering the drawbacks of technology scaling. Furthermore, higher power density and reduced supply voltages make IR drop increasingly challenging in both wire-bond and flip-chip designs. Today, dynamic digital power issues present a major obstacle in achieving design closure within design schedule and budget.

FloorDirector provides an ASIC design solution which enables early stage chip-level dynamic power analysis and implementation-phase optimization, allowing your backend design team to reduce system-level current peaks, dynamic IR drop and digital power grid noise in SoC designs.

FloorDirector works on a post-synthesis netlist, and optimizations are done in the early stages of your backend design flow. This provides designers with a comprehensive system-oriented solution to address the complexity of SoC digital noise and power integrity before physical implementation. As optimizations are performed at the logic design level, design improvements are complementary to improvements made during physical implementation.

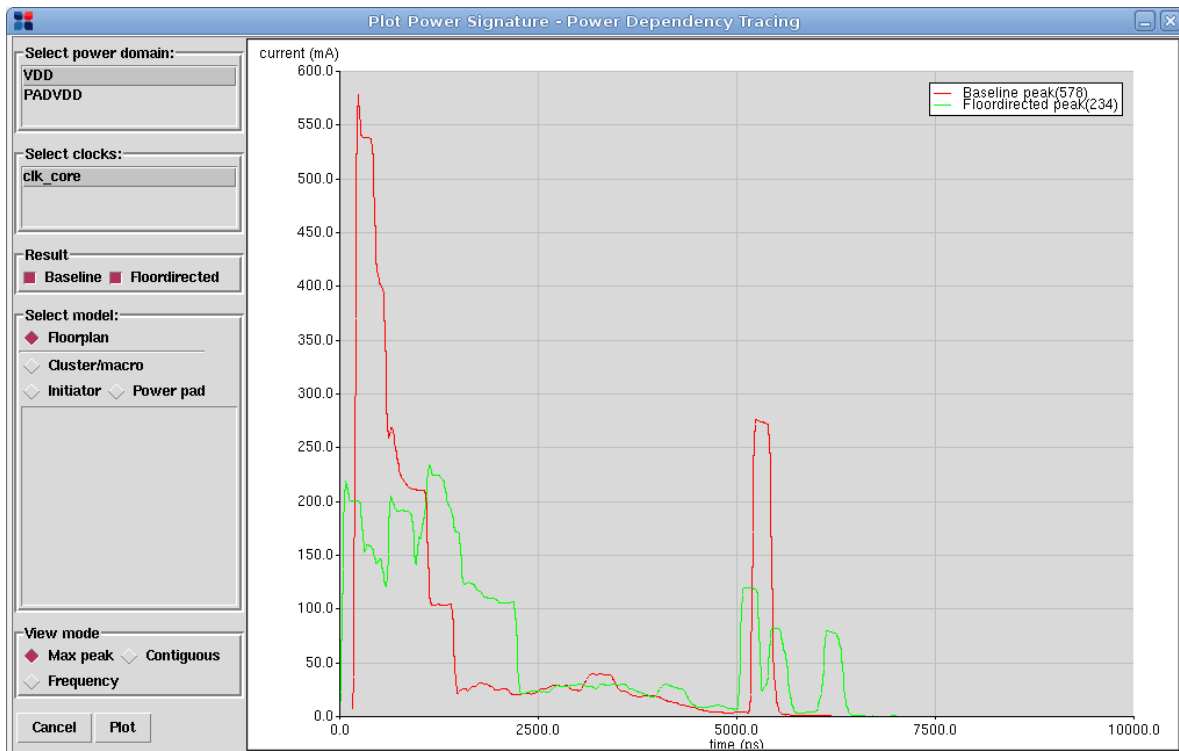


Benefits

Improve Power Integrity
by reducing current peaks

Reduce Digital Noise
at an early stage

Enhance EMI/EMC
using frequency domain analysis



Dynamic supply current analysis and optimization

System-level current peak reduction by FloorDirector (green curve) shows the efficiency of the algorithms compared with the baseline (red curve). All reductions are achieved while maintaining existing timing margins.

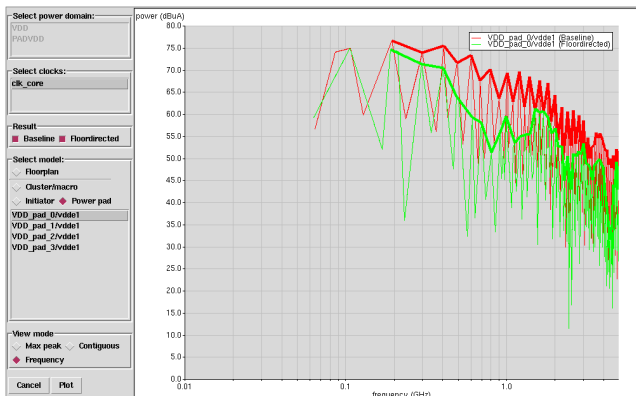
FloorDirector - Early Stage Dynamic Power Optimization

FloorDirector Features

Dynamic Power Shaping™ (DPS)

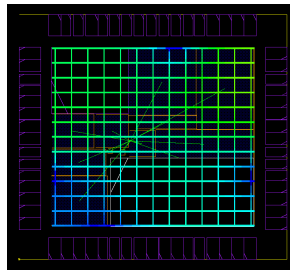
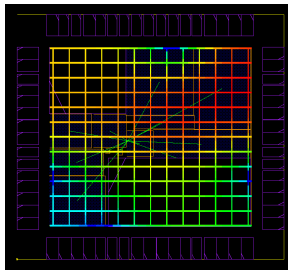
FloorDirector implements a dynamic power analysis engine which reveals current signatures in a design from the post-synthesis stage and onwards. The power analysis further enables power dependency tracing to provide designers with a clear view of power initiators.

The DPS feature builds on this, enabling an automated, proactive, implementation-phase solution to shape current and noise signatures in order to reduce current peaks and power grid noise. This advanced feature lets designers converge on EMI and EMC specifications and improve the performance of noise sensitive on-chip analog circuitry.



Frequency Domain Analysis

Focusing on noise in specific frequency bands can offer significant improvements at design implementation.



Early Rail Analysis

IR drop hotspots shown before and after optimization.

Early Rail Analysis (ERA)

To ensure predictable IC power integrity closure, a clear understanding of the impact of floorplanning on dynamic IR drop and power noise is key. ERA helps designers early in the backend process, when the design is still open to making decisions that matter. Based on a prototype power delivery network (PDN) specification, qualitative early stage what-if floorplanning, PDN and power pad investigations can be performed. FloorDirector ERA is blazingly fast with what-if calculation responses in a few seconds.

FloorDirector's dynamic RC-based ERA engine, combined with its advanced power analysis, strengthens the understanding of power-related issues in the physical design space. This understanding ultimately helps decrease silicon area, and improves routability and yield.

Frequency Domain Analysis (FDA)

Throughout the design exploration process, FDA provides designers with a powerful frequency domain noise analysis capability to assess and visualize noise before and after optimization.

Understanding the impact of design decisions in the frequency domain is particularly useful during the design of mixed-signal SoC sensitive to noise in specific frequency bands. This effectively bridges the existing gap between analog and digital design optimization.

FloorDirector's DPS feature provides significant noise improvements across a broad spectrum of frequencies. Early noise optimization allows for robust, low-noise designs while reducing on-chip decoupling capacitance; thereby saving silicon area and reducing leakage power.



Teklatch provides targeted design automation solutions to the semiconductor industry. With innovations in noise and power integrity optimization, Teklatch is focused on meeting the demands of next-generation semiconductor products.

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